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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/649,411	08/27/2003	Heike Drummer	P2001,0134	5308

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EXAMINER	
CHEN, KIN CHAN	
ART UNIT	**PAPER NUMBER**
1765	

DATE MAILED: 06/09/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/649,411	DRUMMER ET AL.	
	Examiner	Art Unit	
	Kin-Chan Chen	1765	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 May 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) *8-14* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *082703*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election of claims 1-7 in the reply filed on May 17, 2005 is acknowledged. Because applicant did not distinctly and specifically point out the supposed errors in the restriction requirement, the election has been treated as an election without traverse (MPEP § 818.03(a)).

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hirota et al. (US 6,316,329) in view of Nishioka et al. (US 5,489,548) or Vaartstra (US 6,225,237).

In a method for forming a trench mask, Hirota teaches that a first layer may be deposited on the substrate. A second layer (e.g., hardmask) may be deposited on the first layer. The third layer (e.g., photoresist) may be deposited thereon. The third layer may be patterned and used as an etching mask to etch the second layer. The third

layer may be removed the second layer may be used as an etching mask to etch the first layer. A fourth layer of an insulating material may be deposited in the semiconductor substrate. CMP may be performed to remove the fourth layer from the second layer and then to remove the second layer from the upper layer of the first layer (col. 6; Figs. 3A to 3F; col. 10; lines 33-41).

The disclosure of Hirota is not limited to any particular structure but teaches polishing hardmask of any buried structure in which an insulator film or a conductive film is filled up in a trench formed in a substrate. Hence, it would have been obvious to one with ordinary skilled in the art to etch the conventional structures in the art such as a configuration of a plurality of layers including an upper layer having a metal, a middle layer having barium-strontium-titanate or strontium-bismuth-tantalate, and a lower layer having iridium or iridium oxide as claimed. Nishioka (col. 9, TABLE) or Vaartstra (col. 8, lines 4-12) is only relied to show the conventional structure of said configuration of the plurality of layers. Hence, it would have been obvious to one with ordinary skilled in the art to use said configuration of the plurality of layers of in the process of Hirota in order to form a trench isolation structure because it is conventional structure and because it is disclosed by Nishioka or Vaartstra.

The limitations of dependent claims 2-4 have been addressed above and rejected for the same reasons, supra.

The above-cited claims differ from the prior art by specifying well-known features (such as polishing fluid having a solids contents of between 20% and 40% in claim 5; polishing fluid including ammonia in claim 6; polishing fluid having a pH

between 9 and 11 in claim 7) to the art of semiconductor device fabrication. It is the examiner's position that a person having ordinary skill in the art at the time of the claimed invention would have found it obvious to (incorporate) modify the combined prior art by adding any of same well-known features to same in order to planarize a trench isolation structure without deterioration of the device characteristics.

4. Claims 1-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Clevenger et al. (US 6,348,395) in view of Nishioka et al. (US 5,489,548) or Vaartstra (US 6,225,237).

In a method for forming a trench mask, Clevenger teaches that a first layer may be deposited on the substrate. A second layer (e.g., hardmask) may be deposited on the first layer. The third layer (e.g., photoresist) may be deposited thereon. The third layer may be patterned and used as an etching mask to etch the second layer. The third layer may be removed. The second layer may be used as an etching mask to etch the first layer. A fourth layer of an insulating material may be deposited in the semiconductor substrate. CMP may be performed to remove the fourth layer from the second layer and then to remove the second layer from the upper layer of the first layer (col. 8, lines 39-52; Figs. 3A to 3D; col. 9; lines 9-18).

The disclosure of Clevenger is not limited to any particular structure but teaches polishing hardmask of any buried structure in which an insulator film is filled up in a trench formed in a substrate. Hence, it would have been obvious to one with ordinary skilled in the art to etch the conventional structures in the art such as a configuration of

a plurality of layers including an upper layer having a metal, a middle layer having barium-strontium-titanate or strontium-bismuth-tantalate, and a lower layer having iridium or iridium oxide as claimed. Nishioka (col. 9, TABLE) or Vaartstra (col. 8, lines 4-12) is only relied to show the conventional structure of said configuration of the plurality of layers. Hence, it would have been obvious to one with ordinary skilled in the art to use said configuration of the plurality of layers of in the process of Clevenger in order to form a trench isolation structure because it is conventional structure and because it is disclosed by Nishioka or Vaartstra.

The limitations of dependent claims 2-4 have been addressed above and rejected for the same reasons, supra.

The above-cited claims differ from the prior art by specifying well-known features (such as polishing fluid having a solids contents of between 20% and 40% in claim 5; polishing fluid including ammonia in claim 6; polishing fluid having a pH between 9 and 11 in claim 7) to the art of semiconductor device fabrication. It is the examiner's position that a person having ordinary skill in the art at the time of the claimed invention would have found it obvious to (incorporate) modify the combined prior art by adding any of same well-known features to same in order to planarize a trench isolation structure without deterioration of the device characteristics.

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kin-Chan Chen whose telephone number is (571) 272-1461. If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, Nadine Norton can be reached on (571) 272-1465. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

June 6, 2005

Kin-Chan Chen
Primary Examiner
Art Unit 1765

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